Akiho Kawada

Pronouns: she/her/hers
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Homepage: https://akiho-kawada.github.io/

Education

the University of Tokyo, Faculty of Engineering April 2023 – March 2026 (Expected)
the Department of Systems Innovation *Tokyo, Japan*

- Thesis advisor: Prof. Yutaka Matsuo and Prof. Yusuke Iwasawa (Matsuo-Iwasawa Lab)
- Research theme: The Strong Lottery Ticket Hypothesis in Vision Transformers

the University of Tokyo, College of Arts and Sciences April 2021 – March 2023
Natural Sciences I program *Tokyo, Japan*

- Completed foundational courses in the Liberal Arts and Sciences as part of the Natural Sciences I program

Experience

AKARI, Inc December 2022 – March 2024
Machine Learning Engineer/Software Engineer Intern *Tokyo, Japan*

- **ML:** Containerized a cutting-edge segmentation model and its inference systems, and deployed them as a scalable microservice, making it accessible via a REST API for easy integration with existing and future applications.
- **ML:** Fine-tuned some large language models such as Llama 2 and Vicuna, using Kubernetes GPU clusters
- **ML:** Developed some Retrieval Augmented Generation (RAG) services (algorithm side)
- **Software:** Developed and maintained web applications using Typescript, React and NextJS
- **Software:** Developed an advanced application utilizing the OpenAI API for Retrieval Augmented Generation (RAG) to enhance backend data processing and user query responses.

Graduate School of Engineering, the University of Tokyo October 2023 – June 2024
Research Intern *Tokyo, Japan*

- Kosuge Lab, Department of Electrical Engineering and Information Systems, Graduate School of Engineering, the University of Tokyo
- Supervisor: Prof. Atsutake Kosuge
- Conducted RTL design of pre-processing for energy-efficient DNNs and performed FPGA-based validations on it.

Google Summer of Code May 2024 - August 2024 (Expected)
GSoC student/contributor *Remote*

- Project: Transforming the OpenHW High Performance Data Cache into a High Performance Instruction Cache
- Organization: Free and Open Source Silicon Foundation
- Mentors: Prof.Jonathan Balkind, Dr.César Fuguet Tortolero and Ms.Noelia Oliete Escuín
- Extending the high-performance data cache (HPDC) integrated into the CVA6/Ariane core to also function as an instruction cache.

Publications

- **A 250.3mW Versatile Sound Feature Extractor Using 1024-Point FFT 64-ch LogMel Filter in 40nm CMOS**
  Akiho Kawada*, Kenji Kobayashi*, Jaewon Shin, Rei Sumikawa, Mototsugu Hamada, Atsutake Kosuge
  Accepted for presentation at IEEE Asia Pacific Conference On Circuits and Systems (APCCAS) 2024

Skills

Programming Languages/HDL: Verilog/SystemVerilog, Python, C/C++, TypeScript, HTML/CSS

Tools: Vivado, Verilator, PyTorch, Python libraries(numpy, pandas, matplotlib, seaborn, sklearn etc.), Huggingface, OpenCV, Docker, Singularity, Kubernetes, NextJS, React

Language: Japanese(Native), English(CEFR B2), Mandarin Chinese(CEFR C)